

JL7013A Datasheet

Zhuhai Jieli Technology Co.,LTD

Version: 2.0

Date: 2025.01.13

JL7013A Features

CPU

- 32bit Dual-Core DSP
- Maximum speed 160MHz
- 32KB ICache and 16KB DCache
- IEEE754 Single precision FPU
- Mathematical accelerate engine
- Interrupts with 8 priority level

Memory

- On-chip 640KB SRAM
- Support MMU
- Built-In Flash
- SPI PSRAM controller

Clocks

- On-chip 16 MHz clock oscillator
- On-chip 200 kHz lower-temperature-drift clock oscillator
- 24 MHz crystal oscillator
- 32.768 kHz crystal oscillator

DSP Audio Processing

- LDAC, LHDC, SBC, AAC Audio decodes supported for BT audio
- mSBC voice codec supported for BT phone
- Supports MP2, MP3, WMA, APE, FLAC, AAC, MP4, M4A, WAV, AIF, AIFC audio decoding
- Packet Loss Concealment (PLC) for voice processing
- Multi-AMIC Environmental Noise Cancellation (ENC)
- Multi-band DRC limiter
- Multi-band EQ configuration for voice Effects
- Support Hi-Res Audio

Audio Codec

- Two channels 24-bit DAC, SNR ≥ 104 dB
- Four channels 24-bit ADC, SNR ≥ 95 dB
- Audio DAC Sampling rates of

8kHz/11.025kHz/16kHz/22.05kHz/24kHz/

32kHz/44.1kHz/48kHz/64kHz/88.2kHz/

96kHz are supported

- Audio ADC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz are supported
- Support four digital/analog MIC inputs
- Four channels analog audio inputs
- Audio DAC support differential cap-less mode or single-ended mode
- Direct drive 16ohm/32ohm Speaker loading

Bluetooth

- Compliant with Bluetooth V6.0+BR+EDR+BLE specification (DN Q332415)
- Support AoA/AoD direction finding
- Support LE audio BIS/CIS full function
- Meet class1,class2 and class3 transmitting power requirement
- Maximum +9dbm transmitting power
- EDR receiver with minimum -95dBm sensitivity
- Support a2dp\avctp\avdtp\avrcp\hfp\spp\smpl\att\gap\gatt\rfcomm\sdp\l2cap profile bap 1.0.2\pacs 1.0.2\ccp 1.0\mcp 1.0\micp 1.0\vcap 1.0\csip 1.0.1\ascs 1.1\bass 1.0\cap 1.0\hap 1.0\pbp 1.0.1\lmap 1.0\lc3 1.0.1 a2dp 1.4\avctp 1.4\avdtp 1.3\ avrcp 1.6.3\ hfp 1.9\spp 1.2\rfcomm 1.2\pnp 1.3\ hid 1.1.1\sdp core 6.0\l2cap core 6.0

Graphics

- 2D Graphics accelerator
- Support crop, scale, rotation process
- Support multiple data format graphics
- SPI/QSPI and MCU-8080 display driver

Peripherals

- One full speed USB OTG controller
- One SD host controller for eMMC/SD

- Six multi-function 32-bit timers, support capture and PWM mode
- Four UART interface, UART0,UART1&UART2 support DMA
- Two I2C Master/Slave interface
- Four SPI Master/Slave interface
- I2S master/slave interface supports sampling rates from 8kHz to 192kHz
- PDM slave interface supports sampling rates from 8kHz to 192kHz
- QDEC
- Low power CapSense
- 16-channel 10-bit ADC for analog sampling
- 4-channel Motor PWM controller
- 50 Individually programmable and multiplexed GPIO pins
- Up to 12 external interrupt/wake-up source(low power available,can be multiplexed to any I/O)

PMU

- Built-in lithium battery charging manager,up to 200mA charging current

- Built-in LDO and Buck DC-DC converter
- Less than 2uA sleep current
- RTC sleep current is 8uA
- VPWR range : 4.5V to 5.5V
- VBAT range : 2.2V to 4.5V
- IOVDD range : 2.2V to 3.6V
- Conform with IEC 62368-1:2018 certification

Packages

- QFN68(7mm*7mm)

Temperature

- Operating temperature: -40°C to +85°C
- Storage temperature: -65°C to +150°C

Applications

- Bluetooth Smart Watch
- Bluetooth Smart Home
- Bluetooth Intelligent Voice
- Bluetooth Stereo speaker
- Bluetooth TWS speaker
- Bluetooth alarm clock speaker

1 Block Diagram

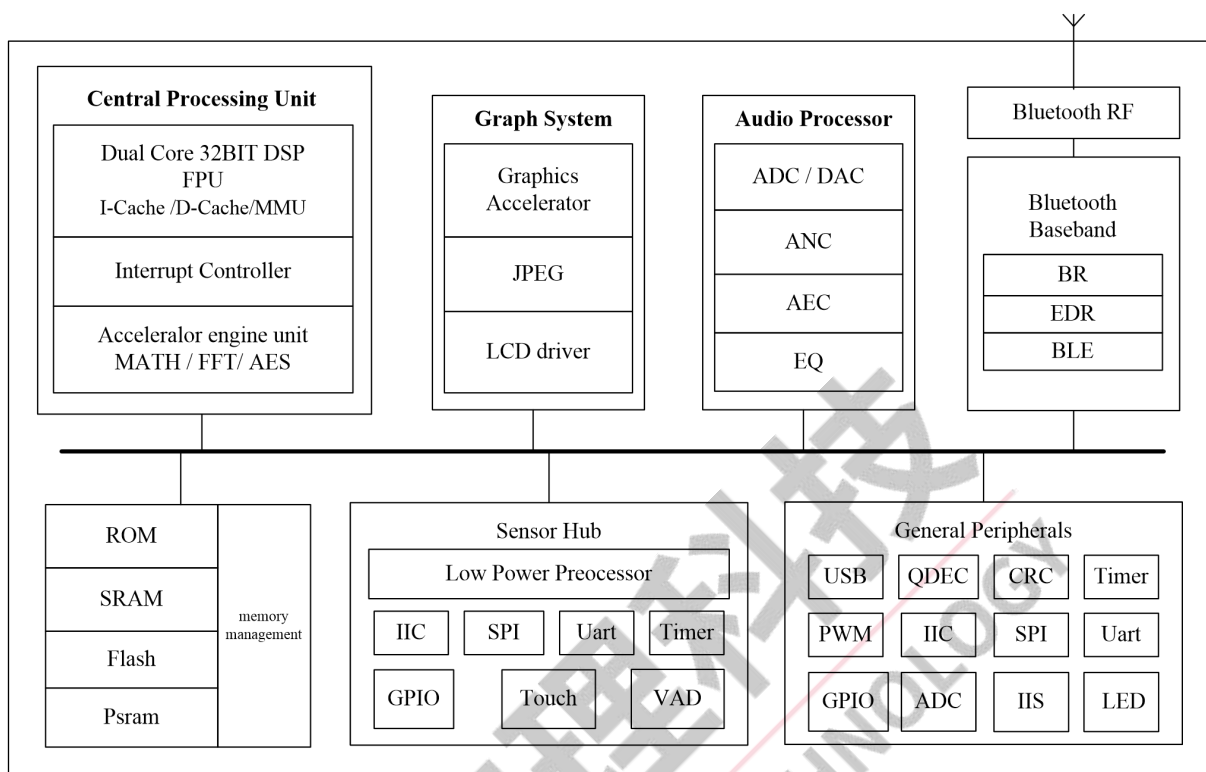


Figure 1-1 JL7013A Block Diagram

2 Pin Definition

2.1 Pin Assignment

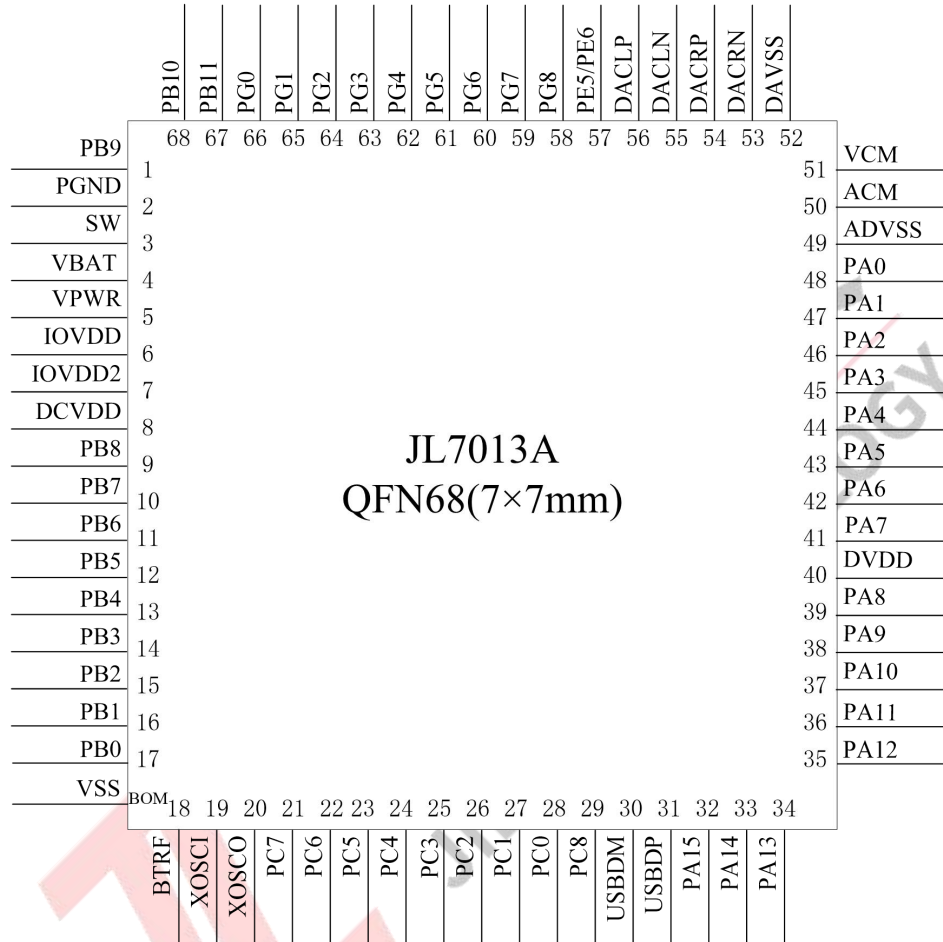


Figure 2-1 JL7013A Package Diagram

2.2 Pin Description

Table 2-1 JL7013A Pin Description

PIN NO.	Name	Type	Function	Other Function
1	PB9	I/O2	GPIO	ADC9:ADC Input Channel 9; SPI4CLKB:SPI4 Clock(B); IIC1_SDA_B:IIC1 SDA(B); Q-decoder2_0:Quadrature decoder2_0;
2	PGND	G		The ground of Buck DC-DC converter;
3	SW	PO		Switch signal of the Buck converter,Connected to inductor;
4	VBAT	P		Battery interface;
5	VPWR (PP0)	PI (I/O)	GPIO	Charging power input; UART0TXB:Uart0 Data Output(B); UART0RXB:Uart0 Data Input(B); CAP1:Timer1 Capture; PWM3:Timer3 PWM Output;
6	IOVDD	PO	Power supply for I/O	Built-in linear voltage regulator output;
7	IOVDD2	PO	Power supply for I/O2	Built-in linear voltage regulator output;
8	DCVDD	P		Internal power;
9	PB8	I/O2	GPIO	CAP4:Timer4 Capture;
10	PB7	I/O2	GPIO	OSC32KI:32.768khz crystal oscillator input;
11	PB6	I/O2	GPIO	OSC32KO:32.768khz crystal oscillator output; PWM2:Timer2 PWM Output;
12	PB5	I/O2	GPIO	LP_Touch4:Low Power Touch Channel 4; IIC1_SDA_A:IIC1 SDA(A); ADC8:ADC Input Channel 8; UART3RXB:Uart3 Data Input(B);
13	PB4	I/O2	GPIO	LP_Touch3:Low Power Touch Channel 3; CLKOUT0:Clock Out0; IIC1_SCL_A:IIC1 SCL(A); UART3TXB:Uart3 Data Output(B); SPI4DIA:SPI4 Data In(A); TMR2:Timer2 Clock Input;
14	PB3	I/O2	GPIO	UART3RXA:Uart3 Data Input(A); SPI4DOA:SPI4 Data Out(A); Q-decoder0_1:Quadrature decoder0_1;

15	PB2	I/O2	GPIO	LP_Touch2:Low Power Touch Channel 2; ADC7:ADC Input Channel 7; UART3TXA:Uart3 Data Output(A); SPI4CLKA:SPI4 Clock(A); CAP5:Timer5 Capture; Q-decoder0_0:Quadrature decoder0_0;
16	PB1	I/O2	GPIO (pull up)	Hold down 0 to reset; LP_Touch1:Low Power Touch Channel 1; ADC6:ADC Input Channel 6;
17	PB0	I/O2	GPIO	LP_Touch0:Low Power Touch Channel 0; TMR4:Timer4 Clock Input;
18	BTRF	RFI		Bluetooth RF antenna interface;
19	XOSCI	I		System Crystal Oscillator Input;
20	XOSCO	O		System Crystal Oscillator Output;
21	PC7	I/O	GPIO (High Voltage Resistant)	
22	PC6	I/O	GPIO (High Voltage Resistant)	ALNK_MCLKB:ALNK Master Clock(B);
23	PC5	I/O	GPIO	SFC1_D2:SFC1 Data2(nor flash); SPI0_DAT2C(2):SPI0 Data2(C); SD0_CLKA:SD0 Clock(A); SPI1DOB:SPI1 Data Out(B); IIC0_SDA_B:IIC0 SDA(B); ALNK_DAT3(B):Audio Link Data3(B); ADC5:ADC Input Channel 5; UART2RXA:Uart2 Data Input(A);
24	PC4	I/O	GPIO	SFC1_DI(D1):SFC1 Data In(nor flash); SPI0_DIC(1):SPI0 Data In(C); SD0_CMDA:SD0 CMD(A); SPI1CLKB:SPI1 Clock(B); IIC0_SCL_B:IIC0 SCL(B); ALNK_DAT2(B):Audio Link Data2(B); ADC4:ADC Input Channel 4; UART2TXA:Uart2 Data Output(A); PWM4:Timer4 PWM Output;
25	PC3	I/O	GPIO	SFC1_CS:SFC1 Chip Select(nor flash); LNA_EN:LNA Enable; SPI0_CSC:SPI0 Chip Select(C); SD0_DATA:SD0 Data(A); SPI1DIB:SPI1 Data In(B); ALNK_LRCK(B):Audio Link Word Select(B); TMR3:Timer3 Clock Input;

26	PC2	I/O	GPIO	SFC1_DO(D0):SFC1 Data Out(nor flash); PA_EN:PA Enable; SPI0_DOC(0):SPI0 Data Out(C); ALNK_SCLK(B):Audio Link Serial Clock(B); TMR1:Timer1 Clock Input;
27	PC1	I/O	GPIO	SFC1_CLK:SFC1 Clock(nor flash); SPI0_CLKC:SPI0 Clock(C); ALNK_DAT1(B):Audio Link Data1(B); TMR5:Timer5 Clock Input; PWMCH1L:Motor PWM Channel1(L);
28	PC0	I/O	GPIO	SFC1_D3:SFC1 Data3(nor flash); SPI0_DAT3C(3):SPI0 Data3(C); ALNK_DAT0(B):Audio Link Data0(B); PWMCH1H:Motor PWM Channel1(H);
29	PC8	I/O	GPIO	SPI2DIB:SPI2 Data In(B);
30	USBDM	I/O	USB Negative Data (pull down)	SPI2DOB:SPI2 Data Out(B); IIC0_SDA_A:IIC0 SDA(A); ADC11:ADC Input Channel 11; UART1RXB:Uart1 Data Input(B);
31	USBDP	I/O	USB Positive Data (pull down)	SPI2CLKB:SPI2 Clock(B); IIC0_SCL_A:IIC0 SCL(A); ADC10:ADC Input Channel 10; UART1TXB:Uart1 Data Output(B);
32	PA15	I/O	GPIO	LCD_D0:MCU8080_D0/RGB_D0; Q-decoder1_1:Quadrature decoder1_1; TMR1CK;
33	PA14	I/O	GPIO	LCD_D1:MCU8080_D1/RGB_D1; Q-decoder1_1:Quadrature decoder1_0; TMR0CK;
34	PA13	I/O	GPIO	LCD_D2:MCU8080_D2/RGB_D2; FPIN1;
35	PA12	I/O	GPIO	LCD_D3:MCU8080_D3/RGB_D3; PWMCH0L:Motor PWM Channel0(L);
36	PA11	I/O	GPIO	LCD_SPID3(A); LCD_D4:MCU8080_D4/RGB_D4; FPIN0;
37	PA10	I/O	GPIO	LCD_SPID2(A); LCD_D5:MCU8080_D5/RGB_D5; FPIN3;
38	PA9	I/O	GPIO	LCD_SPID1/DI(A); LCD_D6:MCU8080_D6/RGB_D6; PWMCH0H:Motor PWM Channel0(H);

39	PA8	I/O	GPIO	LCD_SPID0/DO(A); LCD_D7:MCU8080_D7/RGB_D7; PLNK_DAT1/ANCDE; ALNK_LRCK(A):Audio Link Word Select(A); ADC3:ADC Input Channel 3; UART2RXB:Uart2 Data Input(B);
40	DVDD			Internal power;
41	PA7	I/O	GPIO	LCD_SPICLK(A); LCDCLK:RGB_CLK; ALNK_SCLK(A):Audio Link Serial Clock(A); UART2TXB:Uart2 Data Output(B); TMR0:Timer0 Clock Input;
42	PA6	I/O	GPIO	LCD_RGB_SYNC2; LCD_MCU8080_WR/RD; PLNK_DAT0/ANCDR; SPI2DOA:SPI2 Data Out(A); ALNK_DAT3(A):Audio Link Data3(A); ADC2:ADC Input Channel 2; UART0RXA:Uart0 Data Input(A); CAP0:Timer0 Capture;
43	PA5	I/O	GPIO	LCD_RGB_SYNC1; LCD_MCU8080_WR/RD; PLNK_SCLK/ANCK; SPI2CLKA:SPI2 Clock(A); ALNK_DAT2(A):Audio Link Data2(A); ADC1:ADC Input Channel 1; UART0TXA:Uart0 Data Output(A); PWM5:Timer5 PWM Output;
44	PA4	I/O	GPIO	LCD_RGB_SYNC0; LCD_MCU8080_WR/RD; MIC_BIAS1:MIC1 Bias Output(Built-in resistor); MIC1_N:Different MIC1 Negative; AMUX_B1:Analog Channel B1 input; SPI2DIA:SPI2 Data In(A); ALNK_DAT1(A):Audio Link Data1(A); CAP2:Timer2 Capture;
45	PA3	I/O	GPIO	MICIN1:MIC1 Input Channel 1; MIC1_P:Different MIC1 Positive; AMUX_B0:Analog Channel B0 input; SPI1DOA:SPI1 Data Out(A); ALNK_DAT0(A):Audio Link Data0(A); PWM1:Timer1 PWM Output;

46	PA2	I/O	GPIO	MIC_BIAS0:MIC0 Bias Output(Built-in resistor); MIC0_N:Different MIC0 Negative; AMUX_A1:Analog Channel A1 input; CLKOUT1:Clock Out1; SPI1CLKA:SPI1 Clock(A); ALNK_MCLKA:ALNK Master Clock(A); UART1RXA:Uart1 Data Input(A); CAP3:Timer3 Capture;
47	PA1	I/O	GPIO	MICIN0:MIC0 Input Channel 0; MIC0_P:Different MIC0 Positive; AMUX_A0:Analog Channel A0 input; SPI1DIA:SPI1 Data In(A); UART1TXA:Uart1 Data Output(A); PWM0:Timer0 PWM Output;
48	PA0	I/O	GPIO	MICLDO:Microphone linear voltage regulator output; ADC0:ADC Input Channel 0;
49	ADVSS	G		Audio ADC ground;
50	ACM	P		Audio analog reference bias;
51	VCM	P		Audio analog reference bias;
52	DAVSS	G		Audio DAC ground;
53	DACRN	AO		Right channel audio output negative;
54	DACRP	AO		Right channel audio output positive;
55	DACLN	AO		Left channel audio output negative;
56	DACL P	AO		Left channel audio output positive;
57	PE6	I/O	GPIO	SDPG:SD card power gate;
	PE5	I/O	GPIO	
58	PG8	I/O	GPIO	MICIN2:MIC2 Input Channel 2; MIC2_P:Different MIC2 Positive; AMUX_C0:Analog Channel C0 input;
59	PG7	I/O	GPIO	LCD_SPID3(B); MIC_BIAS2:MIC2 Bias Output(Built-in resistor); MIC2_N:Different MIC2 Negative; AMUX_C1:Analog Channel C1 input; ADC15:ADC Input Channel 15;
60	PG6	I/O	GPIO	LCD_SPID2(B); MICIN3:MIC3 Input Channel 3; MIC3_P:Different MIC3 Positive; AMUX_D0:Analog Channel D0 input; FPIN2;

61	PG5	I/O	GPIO	LCD_SPID1/DI(B); MIC_BIAS3:MIC3 Bias Output(Built-in resistor); MIC3_N:Different MIC3 Negative; AMUX_D1:Analog Channel D1 input; ADC14:ADC Input Channel 14; TMR3CK;
62	PG4	I/O	GPIO	LCD_SPID0/DO(B); SFC_CSB:SFC Chip Select(B); SPI0_CSB:SPI0 Chip Select(B); PWMCH3L:Motor PWM Channel3(L);
63	PG3	I/O	GPIO	LCD_SPICLK(B); TDM_MCLK; SFC_DIB(1):SFC Data In(B); SPI0_DIB(1):SPI0 Data In(B); PWMCH3H:Motor PWM Channel3(H);
64	PG2	I/O	GPIO	TDM_DAT; SFC_DAT2B(2):SFC Data2(B); SPI0_DAT2B(2):SPI0 Data2(B); SD0_CLKB:SD0 Clock(B); PWMCH2L:Motor PWM Channel2(L);
65	PG1	I/O	GPIO	TDM_SYN; SD0_CMDB:SD0 CMD(B); ADC13:ADC Input Channel 13; PWMCH2H:Motor PWM Channel2(H);
66	PG0	I/O	GPIO	TDM_CLK; LVD:Low Voltage Detect; SD0_DATAB:SD0 Data(B); ADC12:ADC Input Channel 12; TMR2CK;
67	PB11	I/O2	GPIO	SPI4DIB:SPI4 Data In(B);
68	PB10	I/O2	GPIO	SPI4DOB:SPI4 Data Out(B); IIC1_SDA_B:IIC1 SDA(B); Q-decoder2_1:Quadrature decoder2_1;
BOM	VSS	G		System ground;

Pin Type	Description	Pin Type	Description
P	Power	I/O	Input or Output (Powered by IOVDD)
PI	Power Input	I/O2	Input or Output (Powered by IOVDD2)
PO	Power Output	I	Input
G	Ground	O	Output
AO	Analog Output	RFI	Radio frequency interface

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1

Symbol	Parameter	Min	Max	Unit
T _{opt}	Operating temperature	-40	+85	°C
T _{stg}	Storage temperature	-65	+150	°C
V _{BAT}	Supply Voltage	-0.3	4.5	V
V _{PWR}	Charger Voltage	-0.3	6	V
V _{IOVDD}	Voltage applied at IOVDD	-0.3	3.6	V
V _{GPIO}	Voltage applied to GPIO	-0.3	IOVDD+0.3	V
V _{HVIO}	Voltage applied to High Voltage Resistant IO	-0.3	Minimum between IOVDD*2 and +5.0V	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

3.2 PMU Characteristics

Table 3-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{BAT}	Voltage Input	2.2	3.7	4.5	V	
V _{PWR}	Charger supply Voltage	4.5	5.0	5.5	V	
Operating mode						
IOVDD	Voltage output	2.0	3.0	3.4	V	V _{BAT} = 4.2V, 10mA loading
	Loading current	—	—	120	mA	IOVDD=3V@V _{BAT} = 4.2V
IOVDD2	Voltage output	1.6	1.8	2.3	V	IOVDD=3V@V _{BAT} = 4.2V
	Loading current	—	—	20	mA	Support for following IOVDD
DCVDD	Voltage output	1.0	1.25	1.4	V	IOVDD=3.0V, 10mA loading
	Loading current	—	—	100	mA	DCVDD=1.25V@IOVDD=3.0v On LDO mode
		—	—	180	mA	DCVDD=1.25V@IOVDD=3.0v On DC-DC mode
DVDD	Voltage output	0.81	1.05	1.26	V	IOVDD=3.0V
V _{LVD}	Voltage input	1.8	2.5	2.5	V	Low-Voltage Detection of IOVDD
Low Power mode						
IOVDD	Loading current	—	—	10	mA	IOVDD=3V@V _{BAT} = 4.2V

3.3 Battery Charge

Table 3-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{PWR}	Charge Input Voltage Range	4.5	5	5.5	V	—
V _{BAT Float}	Battery Charge Termination Voltage	4.15	4.2	4.25	V	VPWR>4.5V
		4.30	4.35	4.40	V	VPWR>4.65V
I _{BAT}	Fast Charge Current	15	—	200	mA	VBAT=4.0V@VPWR=5.0V
I _{END}	Charge Termination Current Threshold	2	—	30	mA	—
V _{Trikl}	Trickle Charge Voltage	—	3.0	—	V	VPWR>4.5V
I _{Trikl}	Trickle Charge Current	1.5	—	30	mA	VBAT<V _{Trikl}

3.4 IO Input/Output Electrical Logical Characteristics

Table 3-4

GPIO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{IL}	Low-Level Input Voltage	-0.3	—	0.3* IOVDD	V	IOVDD = 3.0V
V _{IH}	High-Level Input Voltage	0.7* IOVDD	—	IOVDD+0.3	V	IOVDD = 3.0V
High Voltage Resistant IO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{IL}	Low-Level Input Voltage	-0.3	—	0.3* IOVDD	V	IOVDD = 3.0V
V _{IH}	High-Level Input Voltage	0.7* IOVDD	—	+5V	V	IOVDD = 3.0V
GPIO & High Voltage Resistant IO output characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{OL}	Low-Level Output Voltage	—	—	0.1* IOVDD	V	IOVDD = 3.0V
V _{OH}	High-Level Output Voltage	0.9* IOVDD	—	—	V	IOVDD = 3.0V

3.5 Internal Resistor Characteristics

Table 3-5

Port	Drive Current		Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA0~PA15 PC0~PC5,PC8 PG0~PG8 PE5,PE6	HD1,HD0=0,1	8mA	10K	10K	1. PB1 default pull up 2. USBDM & USBDP default pull down 3. Internal pull-up/pull-down resistance accuracy $\pm 20\%$
	HD1,HD0=1,0	26mA			
	HD1,HD0=1,1	46mA			
PB0~PB11 PC6,PC7 PP0(VPWR)	8mA		10K	10K	
USBDP	4mA		1.5K	15K	
USBDM	4mA		180K	15K	

3.6 Audio DAC Characteristics

Table 3-6

Parameter	MODE	Min	Typ	Max	Unit	Test Conditions
Frequency Response		20	—	20K	Hz	1KHz/0dB 10k ohm loading With A-Weighted Filter
Output Swing	Differential	—	1	—	Vrms	
	Single-ended	—	520	—	mVrms	
THD+N	Differential	—	-70	—	dB	
	Single-ended	—	-70	—	dB	
S/N	Differential	—	104	—	dB	
	Single-ended	—	98	—	dB	
Dynamic Range	Differential	—	104	—	dB	1KHz/-60dB 10k ohm loading With A-Weighted Filter
	Single-ended	—	98	—	dB	
Noise Floor	Differential	—	5.8	—	uVrms	A-Weighted Filter
	Single-ended	—	5.8	—	uVrms	

3.7 Audio ADC Characteristics

Table 3-7

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range	—	94	—	dB	Fsample=44.1kHz,Gain=0dB Fin=1KHz 590mVrms
S/N	—	95	—	dB	Fsample=44.1kHz,Gain=0dB Fin=1KHz 590mVrms
THD+N	—	-75	—	dB	
S/N	—	76	—	dB	Fsample=44.1kHz,Gain=18dB Fin=1KHz 75mVrms
THD+N	—	-73	—	dB	

3.8 BT Characteristics

3.8.1 Transmitter BDR & EDR

Basic Data Rate

Table 3-8

Parameter		Min	Typ	Max	Unit	Test Conditions
RF Transmit Power			7.0		dBm	25°C, Power Supply VBAT=3.7V 2441MHz 4 Layer Board
RF Power Control Range			18.2		dB	
20dB Bandwidth			950		KHz	
In-band spurious Emissions (BQB Test Mode RF_Tx Power=5dBm)	F=F0±1MHz		-22		dBm	
	F=F0±2MHz		-51		dBm	
	F=F0±3MHz		-55		dBm	
	F=F0+/->3MHz		-55		dBm	

Enhanced Data Rate

Table 3-9

Parameter		Min	Typ	Max	Unit	Test Conditions
Relative Power			-2.5		dB	25°C Power Supply VBAT=3.7V 2441MHz 4 Layer Board
$\pi/4$ DQPSK Modulation Accuracy	DEVM RMS		6		%	
	DEVM 99%		11		%	
	DEVM Peak		16		%	
In-band spurious Emissions (BQB Test Mode RF_Tx Power=5dBm)	F=F0±1MHz		-4		dBm	2441MHz 4 Layer Board
	F=F0±2MHz		-34		dBm	
	F=F0±3MHz		-43		dBm	
	F=F0+/->3MHz		-48		dBm	

3.8.2 Receiver BDR & EDR

Basic Data Rate

Table 3-10

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-92		dBm	25°C
Co-channel Interference Rejection			10		dB	
Adjacent Channel selectivity C/I	+1MHz		-4		dB	Power Supply
	-1MHz		-3		dB	VBAT=3.7V
	+2MHz		-39		dB	2441MHz
	-2MHz		-33		dB	DH5
	+3MHz		-45		dB	4 Layer Board
	-3MHz		-28		dB	

Enhanced Data Rate

Table 3-11

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity		-95	-94		dBm	25°C
Co-channel Interference Rejection			10		dB	
Adjacent Channel selectivity C/I	+1MHz		-8		dB	Power Supply
	-1MHz		-8		dB	VBAT=3.7V
	+2MHz		-40		dB	2441MHz
	-2MHz		-33		dB	2DH5
	+3MHz		-45		dB	4 Layer Board
	-3MHz		-27		dB	

3.8.3 BLE

1M Data Rate

Table 3-12

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-97		dBm	25°C Power Supply VBAT=3.7V 2441MHz 4 Layer Board
RF Transmit Power			6.5		dBm	
In-band Spurious Emission	M-N =2MHz			-40	dBm	
	M-N ≥3MHz			-50	dBm	
Modulation Characteristics	Δf1 avg		250		KHz	
	Δf2 99%		200		KHz	
	Δf1avg/Δf2avg		0.9		/	
Carrier Frequency Offset		-10		+10	KHz	
Frequency Drift		-10		+10	KHz	
Frequency Drift Rate		-5		+5	KHz/50us	

2M Data Rate

Table 3-13

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-94		dBm	25°C Power Supply VBAT=3.7V 2441MHz 4 Layer Board
RF Transmit Power			6.5		dBm	
In-band Spurious Emission	M-N =4MHz			-40	dBm	
	M-N =5MHz			-40	dBm	
	M-N ≥6MHz			-50	dBm	
Modulation Characteristics	Δf1 avg		500		KHz	
	Δf2 99%		415		KHz	
	Δf1avg/Δf2avg		0.9		/	
Carrier Frequency Offset		-10		+10	KHz	
Frequency Drift		-10		+10	KHz	
Frequency Drift Rate		-5		+5	KHz/50us	

Long Range

Table 3-14

Parameter	Min	Typ	Max	Unit	Test Conditions
Sensitivity LE 125K(S8)		-104		dBm	VBAT=3.7V,25°C 2441MHz
Sensitivity LE 500K(S2)		-101		dBm	

3.9 ESD Protection

Table 3-15

Parameter	Typ.	Test pin	Reference standard
Human Body Mode	±4KV	All pins	JEDEC EIA/JESD22-A114
Machine Mode	±200V	All pins	JEDEC EIA/JESD22-A115
Charge Device Model	±1KV	All pins	JEDEC EIA/JESD22-C101F
Latch up	±200mA	All GPIO pins	JEDEC STANDARD NO.78E
	1.5xVopmax	All power pins	

Note : 1.5xVopmax = 1.5 times maximum operating voltage.

4 Package Information

4.1 QFN68_7×7mm

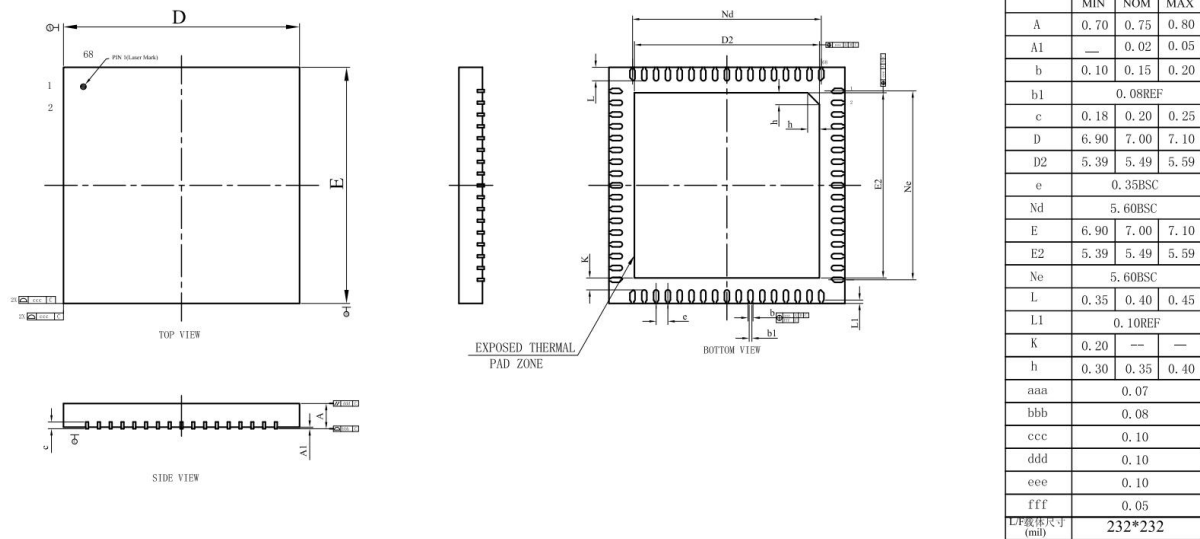
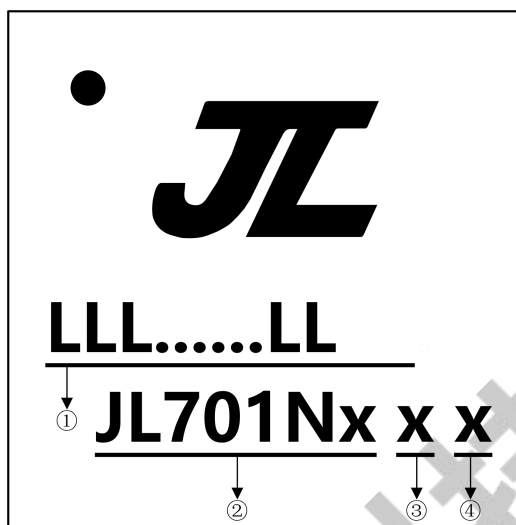


Figure 4-1 JL7013A Package

5 IC Marking Information



① LLL.....LL: LOT No. , It contains 7 to 18 alphanumerics

② JL701Nx: Chip Model

③ x: Built-in flash size

0: No Flash Memory

2: 2Mbit Flash

4: 4Mbit Flash

8: 8Mbit Flash

6: 16Mbit Flash

3: 32Mbit Flash

5: 64Mbit Flash

7: 128Mbit Flash

④ x: Built-in Psram size

Space: No Psram Memory

S: 16Mbit Psram

T: 64Mbit Psram

6 Solder-Reflow Condition

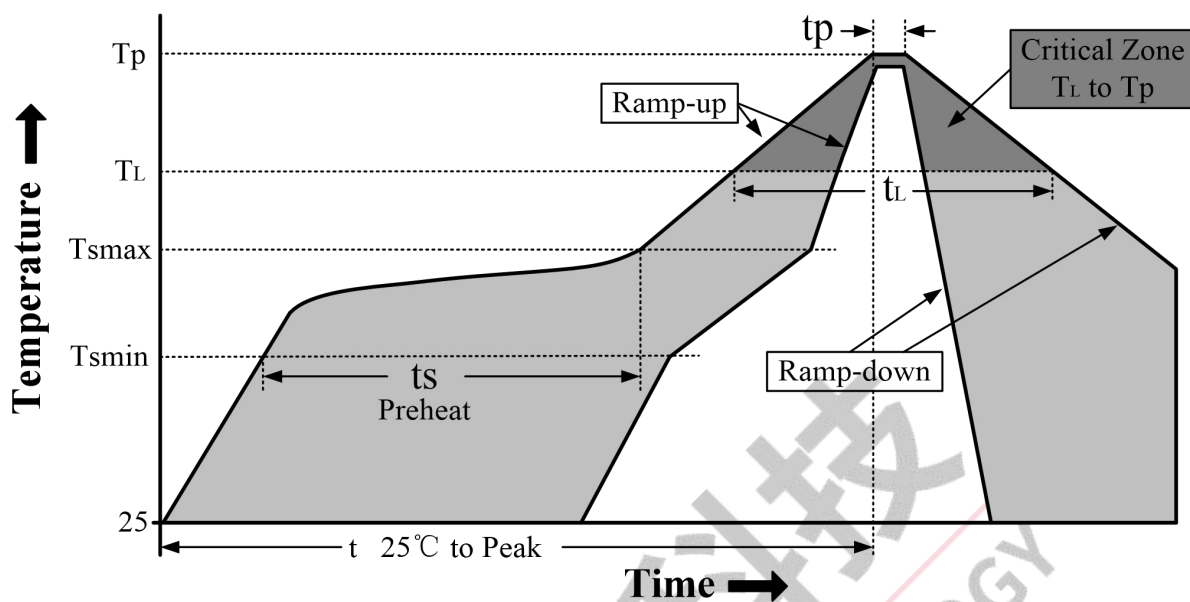


Figure 6-1 Classification Reflow Profile

Classification Profiles

Table 6-1

Profile Feature		Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/ Soak	Temperature Min (T_{smin})	100 °C	150 °C
	Temperature Max (T_{smax})	150 °C	200 °C
	Time (t_s) from (T_{smin} to T_{smax})	60-120 seconds	60-180 seconds
Average ramp-up rate (T_{smax} to T_p)		3 °C/second max	3 °C/second max
Liquidous temperature (T_L)		183 °C	217 °C
Time (t_L) maintained above T_L		60-150 seconds	60-150 seconds
Peak package body temperature (T_p)		See Table 6-2.	See Table 6-3.
Time within 5°C of actual Peak Temperature (t_p)		10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)		6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature		6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

Note 2: Time within 5°C of actual peak temperature (t_p) specified for the reflow profiles is a “supplier” minimum and “user” maximum.

SnPb - Classification Temperature

Table 6-2

Package Thickness	Volume mm ³ < 350	Volume mm ³ ≥ 350
<2.5 mm	240 +0/-5 °C	225 +0/-5 °C
≥ 2.5 mm	225 +0/-5 °C	225 +0/-5 °C

Pb-free - Classification Temperature **Table 6-3**

Package Thickness	Volume mm³ < 350	Volume mm³ 350 - 2000	Volume mm³ > 2000
< 1.6mm	260 °C	260 °C	260 °C
1.6 mm - 2.5mm	260 °C	250 °C	245 °C
> 2.5mm	250 °C	245 °C	245 °C

7 Storage Condition

7.1 Moisture Sensitivity Level

JL7013A is qualified to moisture sensitivity level MSL3 in accordance with JEDEC J-STD-033.

7.2 Storage Alert

1. Calculated shelf life in sealed bag 12 months at $<40^{\circ}\text{C}$ and 90% relative humidity (RH).
2. Peak package body temperature $\leq 260^{\circ}\text{C}$.
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be mounted within 168 hours of factory conditions $\leq 30^{\circ}\text{C}/60\%\text{RH}$ or stored per J-STD-033.
4. Devices require bake before mounting if humidity indicator card reads $> 10\%$ for level 2a-5a devices or $> 60\%$ for level 2 devices when read at $23 \pm 5^{\circ}\text{C}$, or 3a or 3b are not met.
5. Please refer to IPC/JEDEC J-STD-033 for baking procedure if necessary.

8 Revision History

Date	Revision	Description
2022.03.01	V1.0	Initial Release.
2022.04.09	V1.1	Update DAC Characteristics.
2022.05.14	V1.2	Modify the definition of pin49 and pin52; Add IC Marking Information.
2022.06.08	V1.3	Add BLE Parameters.
2022.12.01	V1.4	Modify GPIO parameters.
2023.03.01	V1.5	Modifying Chip Description.
2023.10.19	V1.6	Update BT Features.
2023.12.27	V1.7	Update JL7013A BT_Features(Meet class1 transmitting power requirement); Add ESD protection in Section 3.9; Update BLE Characteristics.
2024.08.09	V1.8	Update Audio & PMU_Features; Update IC Marking Information.
2025.01.13	V2.0	Update Bluetooth Vision.